Q.P. Code: 19MC9102

Reg. No:

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR (AUTONOMOUS)

MCA I Year I Semester Supplementary Examinations November-2020 **COMPUTER ORGANIZATION**

Time: 3 hours Max. Marks: 60

(Answer all Five Units $5 \times 12 = 60$ Marks)

	UNIT-I	
1	a Subtract the following with neat diagram?	6M
	i)1010100-1000011.	
	ii)1001001-(-1000100)	
	b Explain the following i) Decoders ii) Encoders	6M
	OR	
2	a Write about logical operations?	6M
	b Explain about Error detecting codes?	6M
	UNIT-II	
3	a What is memory hierarchy? Write about Main memory	6M
	b Explain about the applications of Logic Micro Operations	6M
	OR	
4	a Explain about Address Sequencing with neat diagram	6M
	b Explain in detail about design of control unit?	6M
	UNIT-III	
5	a Explain about assembler directives?	6M
	b Explain about Data transfer instructions?	6M
	OR	
6	a What are input-output instructions and what are the types?	6M
	b Explain about shift instructions with Example.	6M
	UNIT-IV	
7	a Explain about Peripheral devices?	6M
	b Explain the concept of Pipelining with clear Example?	6M
	OR	
8	a Differentiate between memory mapped I/O and isolated I/O	6M
	b Differentiate between I/O and Memory bus?	6M
	UNIT-V	
9	a Explain about Parallel Processing and its Types?	6M
	b Explain the concept of Pipelining with clear example	6M
	OR	
10	a Explain about vector processing?	6M
	b Explain about Array processors?	6 M

*** END ***